



Semiconductor

Design Powerhouses

India's ER&D Bet
Beyond Chip Fabrication

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Executive Summary

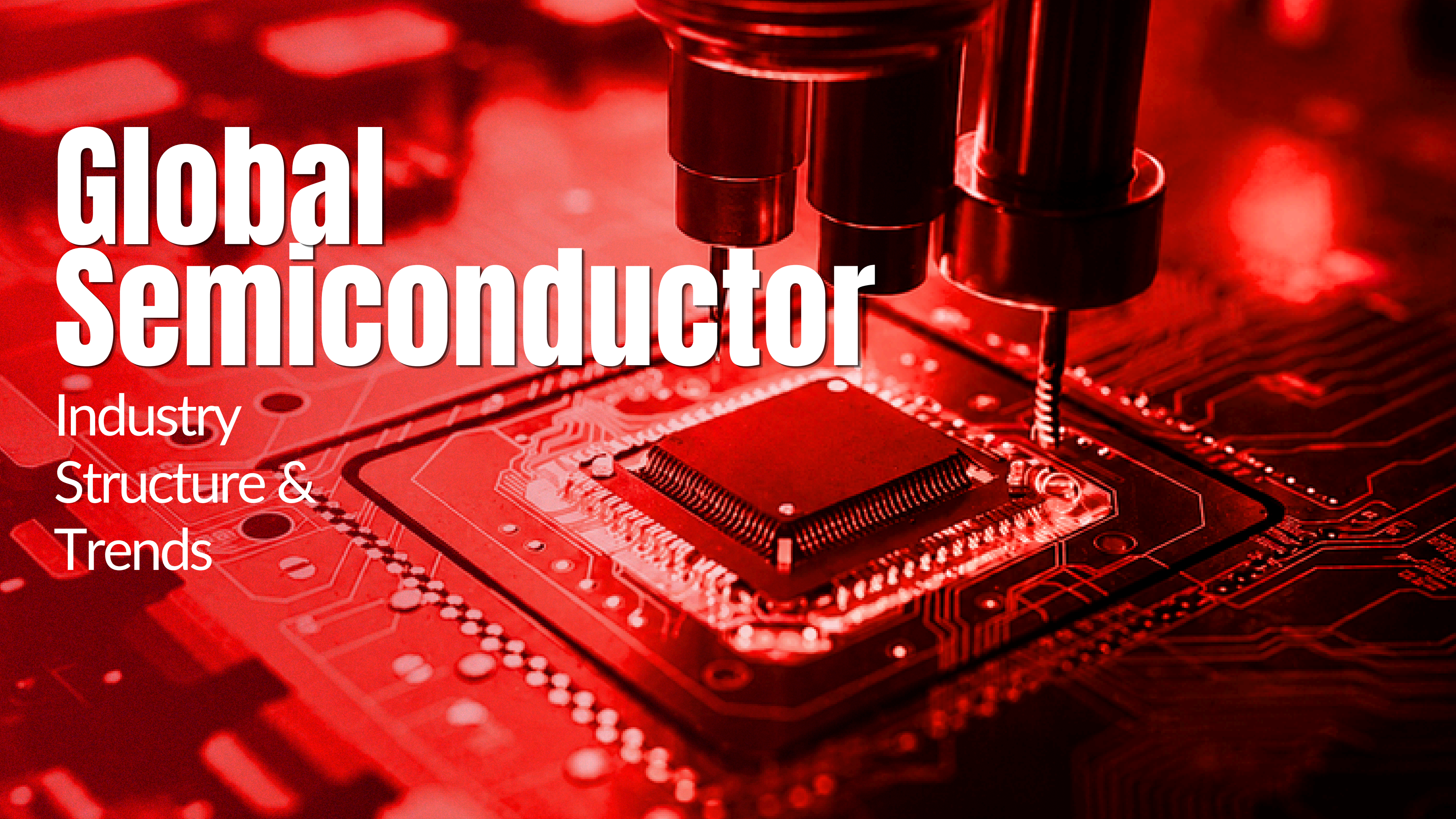
The global semiconductor industry is undergoing structural changes driven by supply chain diversification, increasing engineering complexity, and rising demand for advanced computing systems. India, which accounts for more than 20 percent of global chip design talent, has emerged as a prominent location for semiconductor engineering and global capability center operations. While fabrication infrastructure in India is in progress to develop, the country has established a significant presence in chip design, verification, embedded systems, firmware, and semiconductor software development.

The global semiconductor market reached approximately USD 629 billion in 2026 and is projected to exceed USD 1 trillion by 2035, growing at a compound annual growth rate of approximately 5.3 percent. Key demand segments include automotive electronics, connectivity infrastructure, data center systems, and advanced processors. Semiconductor engineering expenditure is estimated at USD 80 to 90 billion annually and continues to increase with rising product complexity.

This report examines the semiconductor sector in India's engineering R&D ecosystem. It assesses the expansion of semiconductor engineering activities in India, the role of multinational semiconductor firms, the operational position of GCCs within the semiconductor value chain, and the factors supporting India's participation beyond fabrication. The report also reviews talent availability, policy support, regional semiconductor clusters, investment patterns, operational constraints, and expected developments between 2026 and 2035.

Key Findings

- India hosts more than 125,000 semiconductor engineers across chip design, verification, firmware, and embedded systems functions.
- Global semiconductor firms including **Intel, Qualcomm, NVIDIA, AMD, Texas Instruments, Micron Technology, and NXP Semiconductors** operate semiconductor engineering centers in India.
- India's engineering R&D GCC revenue is projected to exceed USD 30 billion by FY2030, with semiconductor engineering representing a growing share.
- The India Semiconductor Mission has committed USD 10 billion toward semiconductor ecosystem development.
- Bengaluru, Hyderabad, Pune, and Chennai account for more than 85 percent of India's semiconductor engineering workforce.
- Engineering R&D participation provides a scalable entry point into the semiconductor value chain before large-scale fabrication capacity is established.
- Automotive semiconductor engineering, accelerator design, and edge computing are projected to remain major growth segments within India's semiconductor sector.

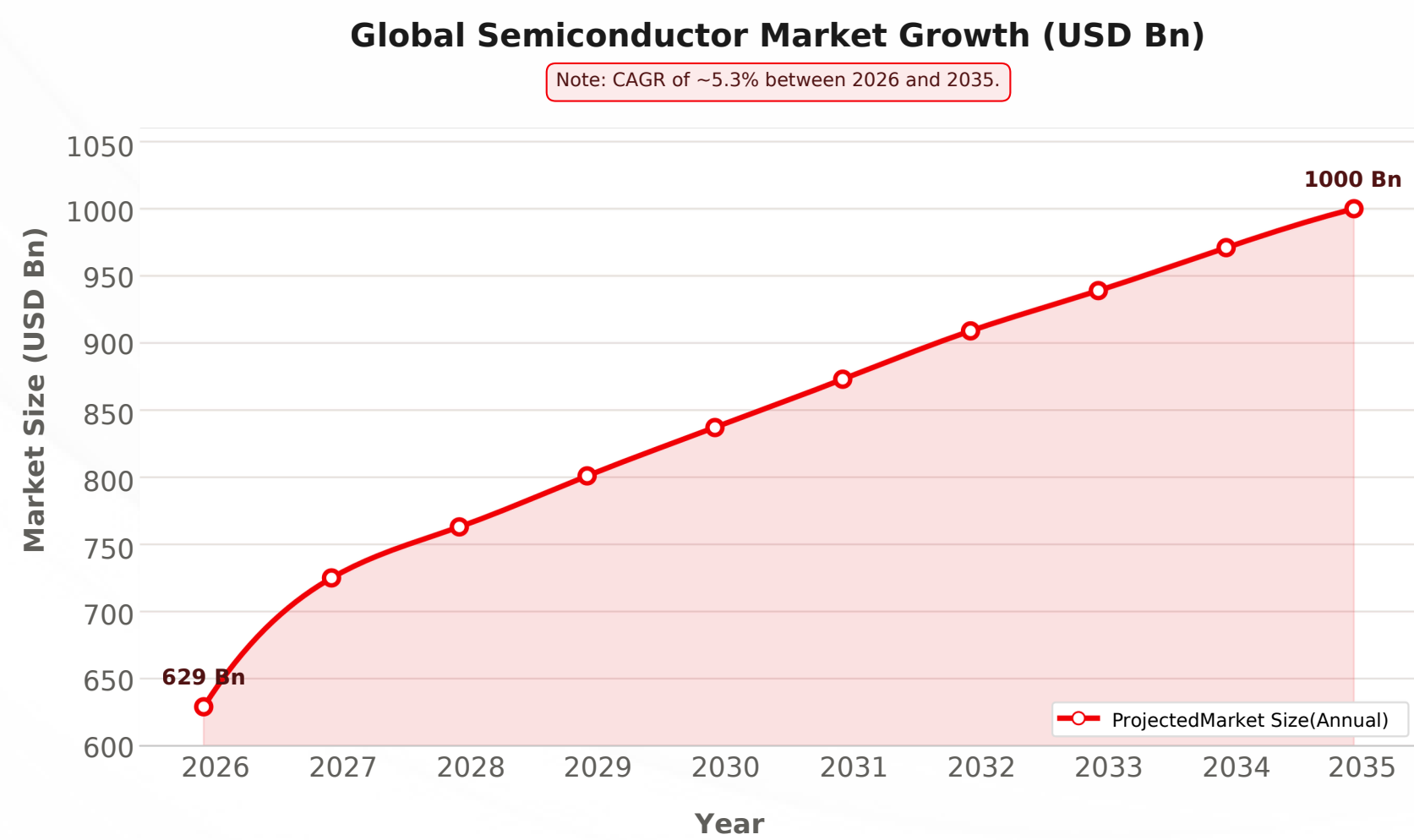


Global Semiconductor

Industry
Structure &
Trends

1.1 Market Structure & Scale

The semiconductor industry is organized across a horizontally and vertically segmented value chain. At the market level, the sector was valued at USD 629 billion in 2026, with logic chips (microprocessors, GPUs, FPGAs, and ASICs) representing the largest category at approximately 35 percent of total revenue. Memory semiconductors account for a further 25 percent, while analog, discrete, and optoelectronic devices constitute the remainder.



The top five semiconductor firms by revenue (Intel, Samsung Semiconductor, TSMC, Qualcomm, and SK Hynix) collectively account for approximately 40 percent of global industry revenue. The sector is capital-intensive at the fabrication stage, with advanced logic fabrication facilities (fabs) requiring USD 15 to 25 billion per plant and technology nodes advancing toward sub-2 nm process geometries.

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1.2 Shift from Manufacturing to Design-Led Value Creation

The semiconductor industry has undergone a structural shift from manufacturing-led competitiveness to design- and innovation-driven value creation. Today, over 50–60% of semiconductor R&D spending is concentrated in design, verification, and embedded software.

Advanced fabrication facilities now require **USD 15–25+ billion per fab**, while semiconductor design and R&D centers typically require **USD 200–500 million**, creating a strong economic case for distributed engineering models.

Three trends are accelerating this shift:



Fabless and fab-lite models

Fabless companies now generate 35%+ of global semiconductor revenue, driving demand for global engineering talent.



Rising design complexity

Advanced SoC design costs have increased from ~USD 40M (28nm) to USD 500M+ (5nm).



Software-defined hardware

Software now accounts for up to 40% of semiconductor development effort.

As a result, the semiconductor value chain is increasingly design-led, making access to large engineering ecosystems a key competitive factor.

1.3 Semiconductor Value Chain

VALUE CHAIN STAGE	KEY ACTIVITIES	REPRESENTATIVE FIRMS	INDIA PARTICIPATION
IP Licensing	Architecture design, ISA licensing	ARM, RISC-V Foundation	Moderate and growing
Chip Design	RTL design, logic synthesis, physical design	Qualcomm, AMD, NVIDIA, Apple	Significant (20%+ talent)
Verification & Validation	Functional simulation, emulation, DFT	Broadcom, Marvell, MediaTek	High concentration
EDA & Tools	Design automation, modeling software	Synopsys, Cadence, Mentor	R&D centers present
Fabrication (Foundry)	Wafer manufacturing, process technology	TSMC, Samsung, Intel Foundry	Nascent (ISMC, Micron ATMP)
OSAT/Packaging	Assembly, testing, and advanced packaging	ASE, Amkor, JCET	Early stage
Embedded Software	Firmware, BSP, device drivers, RTOS	Renesas, NXP, STMicroelectronics	Large and mature

1.4 Geopolitical Shifts

US export controls imposed between 2019 and 2024 have restricted the transfer of advanced semiconductor technology to China, prompting a reorganization of global supply chains. The US CHIPS and Science Act (2022) allocated USD 52.7 billion for domestic semiconductor manufacturing and R&D. The EU Chips Act (2023) targeted EUR 43 billion in investment. Japan, South Korea, and Taiwan have introduced parallel incentive structures. India's response, through the India Semiconductor Mission, positions the country as an alternative destination for diversified engineering and manufacturing investment.

1.5 Global Talent Shortages

The World Semiconductor Trade Statistics and multiple industry assessments have identified a structural shortfall in semiconductor engineering talent across the United States, Europe, and East Asia. The US alone is estimated to require over 90,000 additional semiconductor workers by 2030 to meet projected demand. Germany, Japan, and South Korea face comparable deficits relative to planned capacity expansions. This structural shortage is a direct demand driver for India's engineering talent pool.



Expanding Beyond Fabrication

India's
Semiconductor
Strategy

2.1 The Fabrication Constraints

Advanced semiconductor fabrication requires sustained capital expenditure at a scale and consistency that few nations have matched. A single leading-edge logic fab (sub-5nm) requires USD 15 to 25 billion in construction capital, USD 1 to 3 billion annually in operating costs, a continuous supply of ultrapure materials and chemicals (largely import-dependent), and a gestation period of 5 to 7 years from site selection to volume production. India currently lacks the full ecosystem of specialty chemicals, ultra-high purity gases, lithography support, and precision equipment supply chains required for leading-edge fabrication.

The India Semiconductor Mission has approved projects for fabrication at mature nodes (28 nm and above) and ATMP (assembly, testing, marking, and packaging) capacity. These are structurally important for supply chain resilience and import substitution, but they do not position India for the highest-value segments of semiconductor manufacturing in the near term.

2.2 The ER&D Entry Point

Engineering R&D is capital-light relative to fabrication, scalable incrementally, and dependent primarily on human capital. India's established engineering talent base, its existing GCC infrastructure, and its cost structure make ER&D the most viable near-term pathway for expanding semiconductor sector participation. ER&D operations also generate intellectual property, engineering capability, and process knowledge that compound over time and lay the groundwork for higher-complexity work.

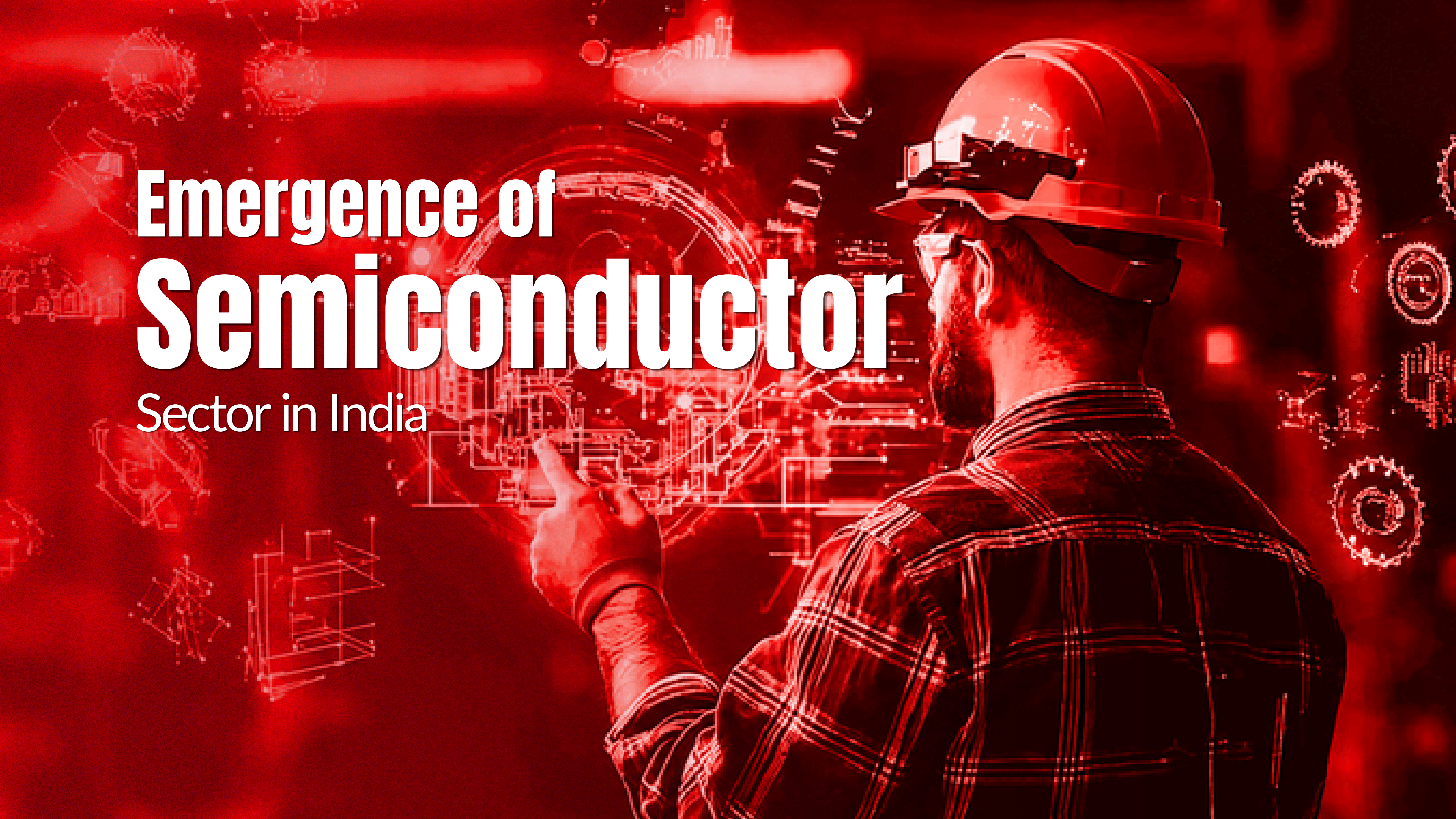
PARAMETER	FABRICATION-LED APPROACH	ER&D-LED APPROACH
Capital Requirement	USD 10 to 25 billion per facility	USD 50 to 300 million per center
Gestation Period	5 to 7 years to volume production	12 to 24 months to full operations
Technology Risk	High (node obsolescence, equipment dependency)	Moderate (talent and process-driven)
India Readiness	Low to Moderate (ecosystem gaps)	High (established talent and infrastructure)
Value Chain Position	Manufacturing: upstream in supply chain	Design; contributes to product definition
IP Generation	Process IP (limited design IP)	Design IP, architecture, software
Scalability	Limited by capital and infrastructure	Scalable through talent formation
Employment Intensity	Moderate (automation-intensive)	High (engineer-intensive)

2.3 India's Design GCC-Led Opportunity

India's participation in the fabless value chain is already substantive. Indian engineering centers contribute to chip architecture, RTL design, physical design, functional verification, VLSI design, and embedded software for semiconductor products sold globally. The next phase of this participation involves deeper ownership of design blocks, subsystem leadership, and product-level engineering responsibility rather than supporting or execution-only roles.

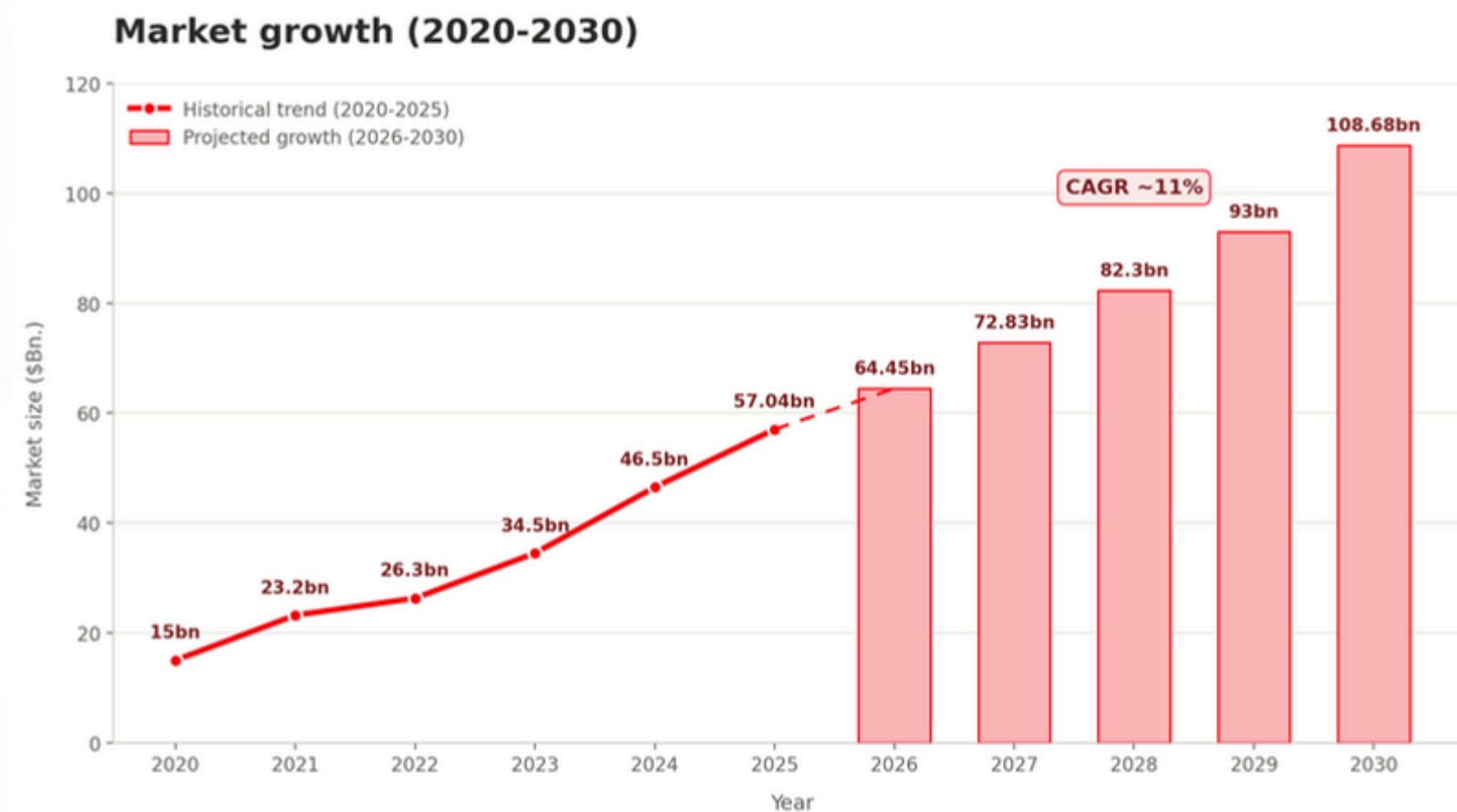
Emergence of Semiconductor

Sector in India



3.1 Market Outlook

India's semiconductor industry is shifting from a primarily consumption-driven market toward a global hub for design, R&D, and manufacturing support capabilities. As per our research, the market experienced a sharp upward trajectory from 2020 to 2025, with the market size effectively more than tripling from 15.0 billion to 57.04 billion in those five years and is forecast to nearly double to USD 108.68 billion by 2030, growing at a CAGR of ~11%, which exceeds global growth rates.

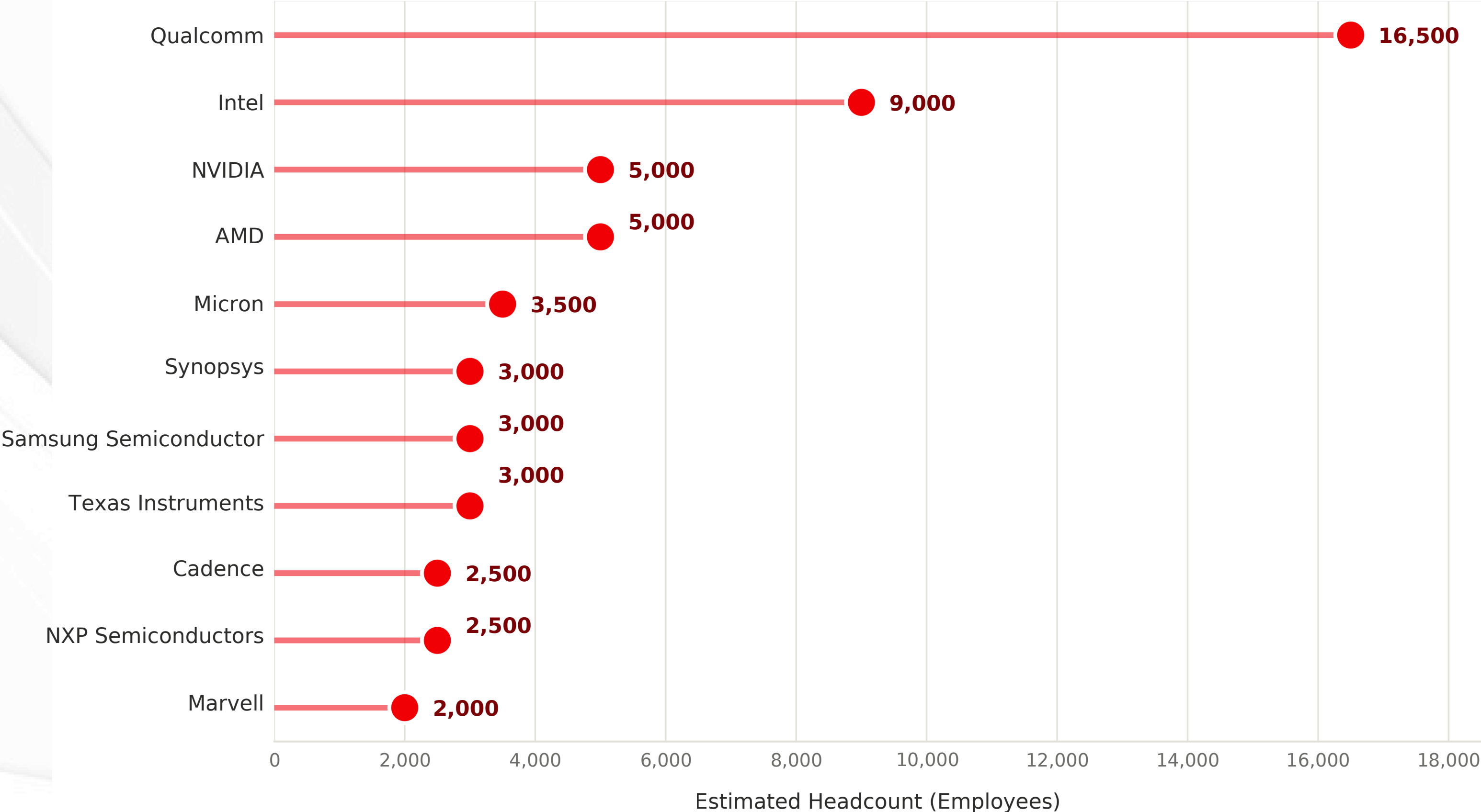


3.2 Corporate Presence and Operational Scope

India has become a strategic hub for semiconductor GCCs, with global firms establishing large engineering centers across Bengaluru, Hyderabad, Pune, and Noida. These centers now contribute to core chip design, verification, embedded software, EDA tools, AI hardware, and automotive semiconductors. Their role has evolved from support functions to owning full product modules and leading global programs. With growing policy support and investments in packaging, testing, and validation, India's footprint is expanding from design-led R&D to broader semiconductor value-chain participation.

Estimated India Headcount of Major Semiconductor GCCs

Lollipop view — ranked by estimated employee headcount



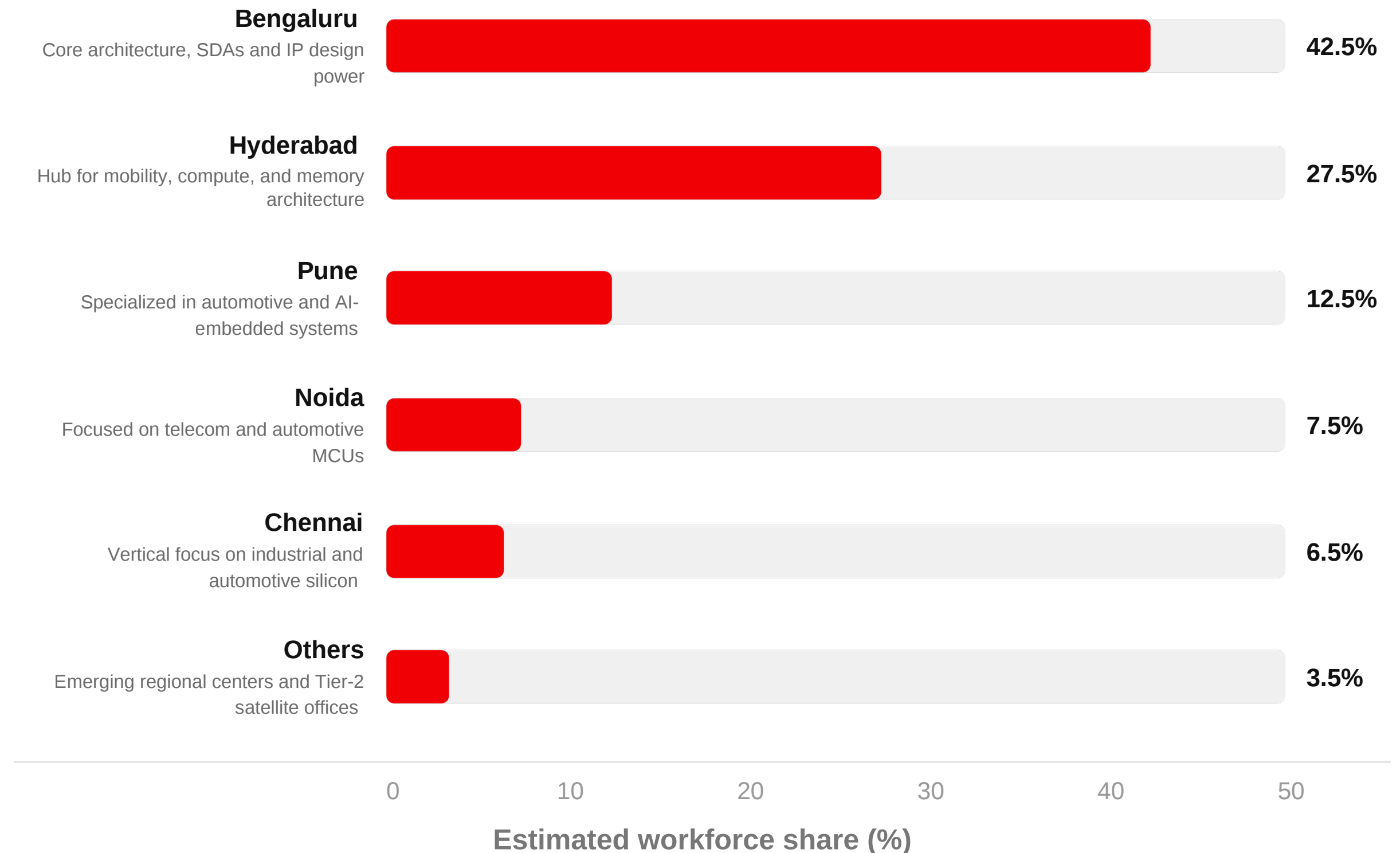
The chart identifies Qualcomm as the largest employer in this segment within India, followed by Intel. Together, these firms represent a significant portion of the core engineering talent focused on modern design, SoC architecture, and platform software.

3.3 Geographic Distribution

Bengaluru accounts for the largest share of India's semiconductor R&D workforce, estimated at 40 to 45 percent of total headcount. The city hosts the Indian centers of Intel, Texas Instruments, ARM, Broadcom, and several EDA companies. Hyderabad has emerged as the second-largest hub, with Qualcomm, AMD, NVIDIA, and Micron operating major centers. Pune is home to NVIDIA's automotive engineering operations and several embedded systems centers. Chennai and Noida serve as secondary hubs for specific verticals, including automotive (Renesas, NXP Noida) and telecom semiconductor design.

Geographic distribution & strategic roles in India's semiconductor R&D

Estimated workforce share by city (%)



3.4 Engineering Specialization Areas

• Chip Design and Verification

Chip design activities in India span the full front-end design flow, including architecture definition, RTL coding, logic synthesis, static timing analysis, and formal verification. Functional verification, which is typically the most labor-intensive phase of modern chip development (often consuming 60 to 70 percent of total engineering effort), is heavily concentrated in India. Companies such as Qualcomm, AMD, and Broadcom rely on Indian centers for verification at scale.

• AI Accelerator Engineering

The demand for AI-specific hardware has generated a new engineering category at the intersection of chip design and software. India centers at NVIDIA, Qualcomm, and several startups (SiPearl, d-Matrix, and Untether AI India teams) are involved in neural processing unit design, AI compiler development, and accelerator architecture. This is among the highest-growth segments within India's semiconductor engineering base.

• Embedded Systems and Firmware

India has a large and mature embedded engineering community. Firmware development, BSP (Board Support Package) engineering, device driver development, and real-time operating system (RTOS) porting are established competencies. The automotive, industrial, and consumer electronics sectors drive sustained demand for embedded firmware engineers, with centers at NXP, Renesas, STMicroelectronics, and Bosch operating in India.

• Automotive Semiconductors

Automotive semiconductor engineering is the fastest-growing vertical in India's semiconductor GCC sector. The increasing electronic content per vehicle (estimated at USD 600 to 800 for internal combustion engine vehicles and USD 2,000 to 3,500 for electric vehicles) has driven semiconductor demand from automotive OEMs and their Tier 1 suppliers. India centers at NXP, Renesas, Continental Automotive, Bosch, and TE Connectivity focus on AUTOSAR-compliant software, functional safety (ISO 26262), vehicle networking (CAN, LIN, and Ethernet), and advanced driver assistance system (ADAS) chip design.

India's Position in the Global ER&D Landscape

RESEARCH

Innovation

Discover

Analysis

Experiments

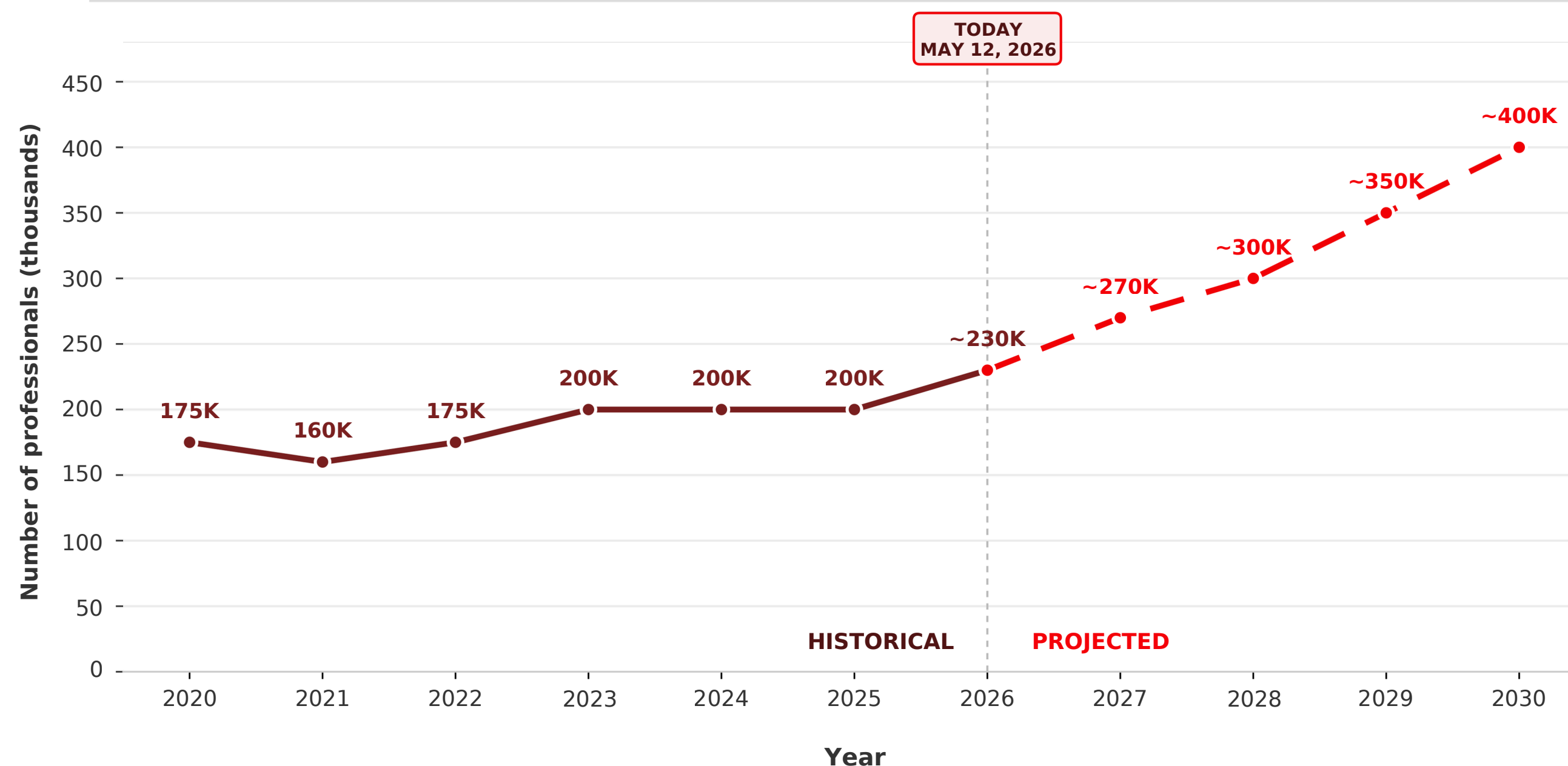


4.1 Talent Scale & Pipeline

India produces approximately 1.5 million engineering graduates annually, with a substantial proportion in electronics, electrical engineering, computer science, and related disciplines. The VLSI and embedded systems engineering pipeline is supported by approximately 400 colleges offering specialized courses, a network of IITs, NITs, and state technical universities, and a growing number of industry-academic programs in semiconductor design. The Indian Institute of Technology network has produced a disproportionate share of senior semiconductor engineers employed globally.

INDIA SEMICONDUCTOR TALENT SUPPLY (2020-2030)

PROJECTED PROFESSIONAL GROWTH ACROSS THE DECADE



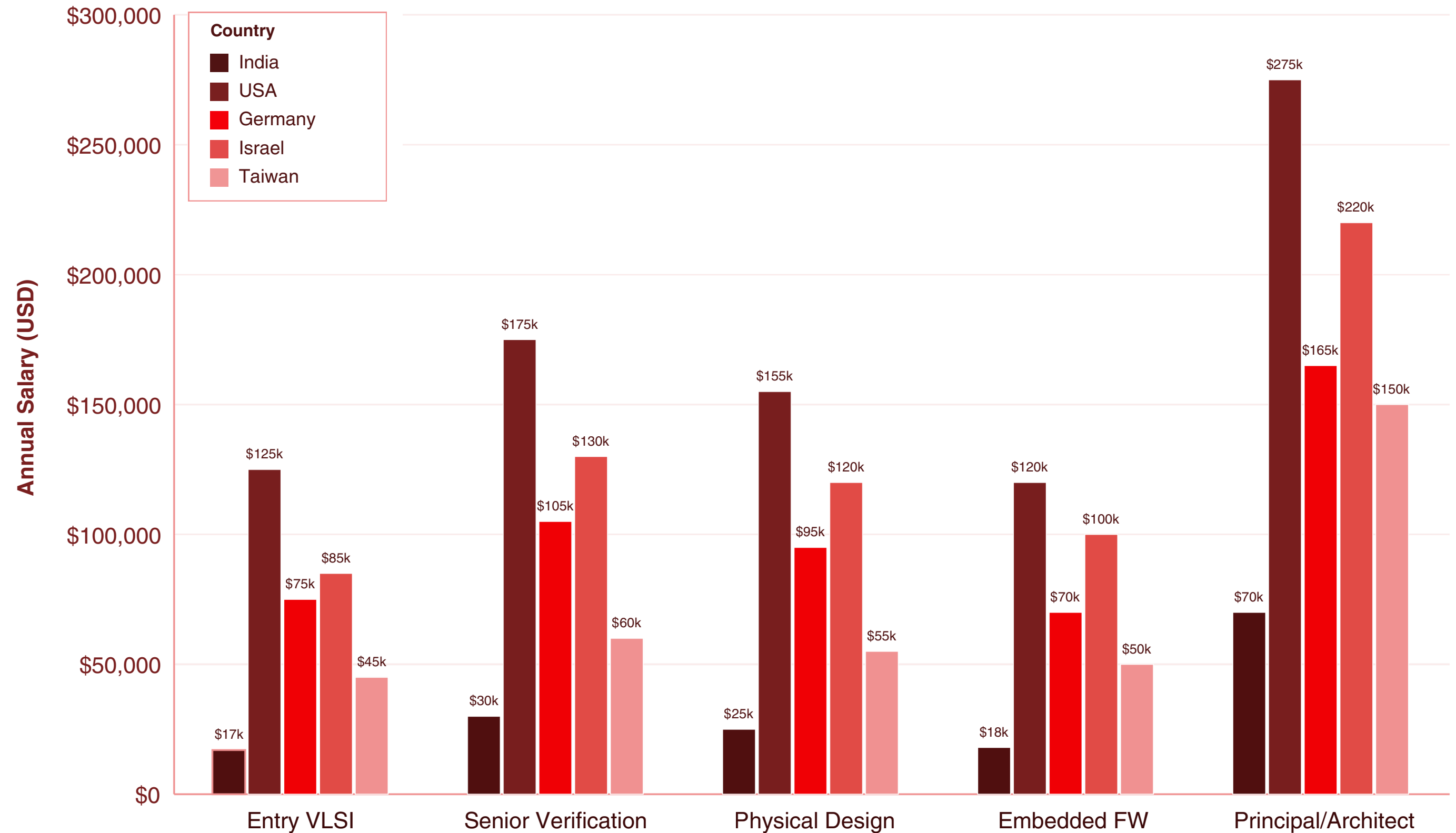
Source: Quess Corp

India's semiconductor talent pool is projected to grow steadily from ~180,000 professionals in 2020 to nearly 400,000 by 2030, reflecting sustained expansion of the design and engineering workforce. This growth signals a strengthening long-term talent pipeline to support increasing global semiconductor R&D demand.

Global Semiconductor Engineering Salary Comparison

4.2 Comparative Cost Structure

This chart illustrates the significant salary disparity across global semiconductor markets, highlighting that U.S. salaries are approximately 4-15x higher than those in India for comparable roles. While India offers a massive cost advantage for entry-level and specialized engineering, the gap is most pronounced at the principal/architect level, where the U.S. remains the highest-paying market globally.



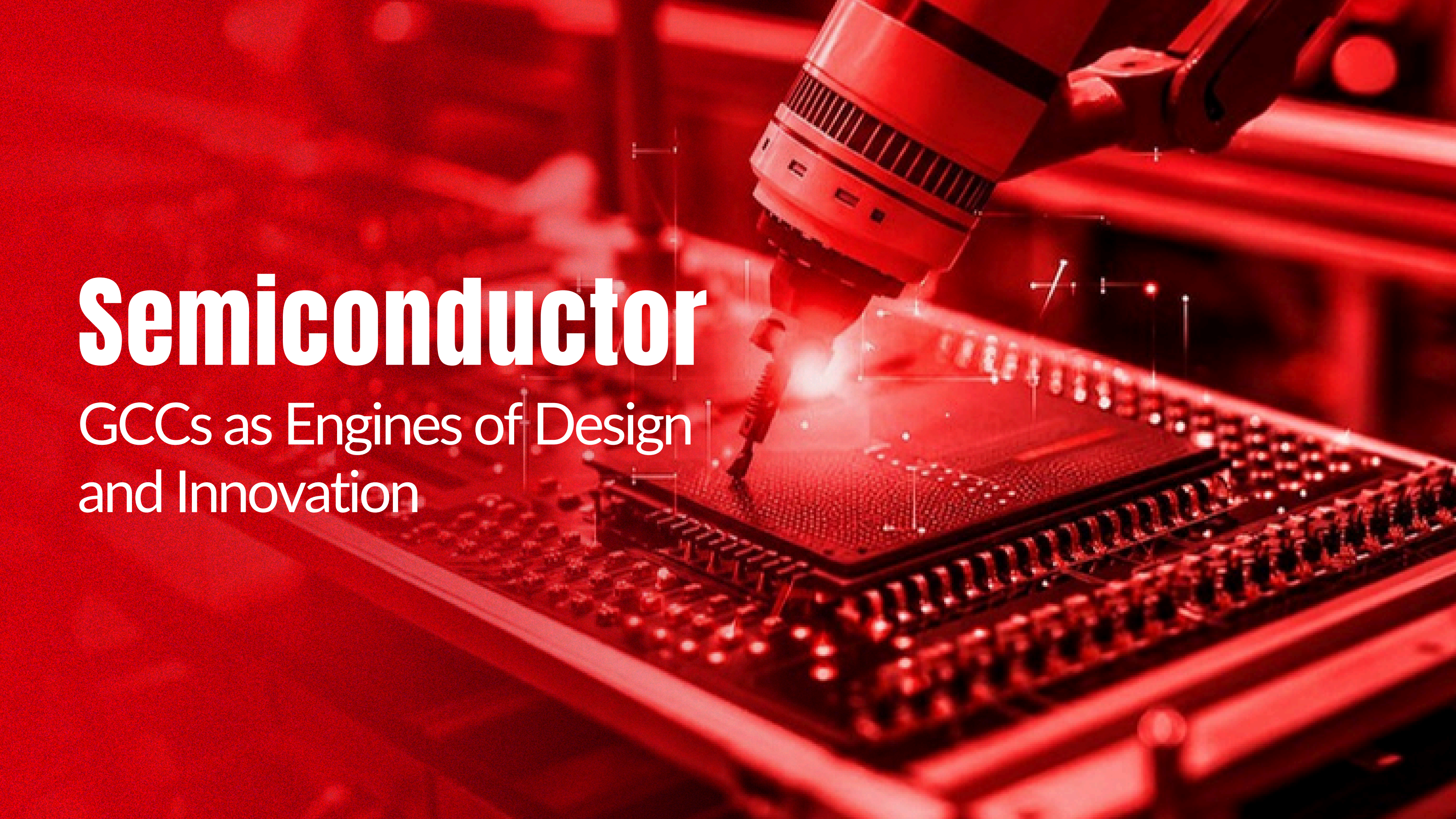


4.3 Engineering Depth

Beyond cost arbitrage, India's semiconductor engineering community has developed expertise depth that is now a standalone competitive factor. Indian centers hold a growing share of patents in areas such as modern algorithms, SoC architecture, and design verification methodology. Qualcomm India holds thousands of patents filed from its Hyderabad center. Texas Instruments India has contributed to analog and mixed-signal design IP for over three decades. The transition from execution to innovation is observable in patent filing trends, standards body participation, and the emergence of semiconductor startups founded by engineers trained in Indian GCCs.

4.4 Time Zone & Operational Advantages

India's time zone (UTC+5:30) provides a 9.5-hour overlap with Central European time and a 10.5 to 13.5-hour offset from US West Coast time, supporting a follow-the-sun engineering model that accelerates product development cycles. For semiconductor firms with design centers in California, Israel, and the UK, India centers complete simulation runs, review results, and prepare engineering documentation overnight relative to US operating hours, compressing design iteration cycles.

The background image is a close-up of a semiconductor manufacturing process. A robotic arm with a welding torch is positioned over a circuit board, creating a bright light at the point of contact. The entire scene is bathed in a deep red light, giving it a high-tech, industrial feel. The text is overlaid on the left side of the image.

Semiconductor

GCCs as Engines of Design
and Innovation

5.1

Operating Model Framework

MODEL TYPE	CHARACTERISTICS	INDIA GCC ROLE	VALUE GENERATED
Execution Center	Defined scope, remote delivery, metrics-based	RTL implementation, documentation, testing	Cost efficiency, capacity
Engineering Partner	Shared ownership, cross-site teams	Subsystem design leads, verification ownership	Speed, scale, engineering depth
Innovation Hub	Product roadmap input, IP generation	Architecture, patent filing, standards work	IP creation, competitive differentiation
Center of Excellence	Global process owner for a domain	Verification CoE, embedded SW CoE	Process standardization, quality

5.2

R&D Cost Reduction

Semiconductor firms operating GCCs in India report effective R&D cost reductions of 40 to 60 percent for equivalent engineering functions relative to comparable US or European operations. This cost differential enables firms to expand the total volume of engineering work without proportionate budget increases, effectively extending the engineering capacity available per product cycle. For chip design programs where verification engineering is the dominant cost, India-based verification teams provide a particularly significant cost lever.

5.3

Product Development Acceleration

Distributed engineering models with India GCCs at scale accelerate product development through parallel workstreams and continuous engineering cycles. AMD and Qualcomm have publicly noted the role of Indian teams in reducing time-to-tapeout for complex SoC designs. NVIDIA's India center contributes to both hardware design and software stack development, enabling simultaneous advancement of hardware and software deliverables.

5.4

Supply Chain & Resilience Benefits

The concentration of advanced semiconductor engineering in a small number of locations (Silicon Valley, Hsinchu, and Seoul) represents a concentration risk that India-based GCCs partially mitigate. Engineering continuity, documentation ownership, and knowledge distribution across India centers provide resilience against facility disruptions, talent shortfalls in specific geographies, and geopolitical restrictions on technology transfer to other regions.

Policy Ecosystem

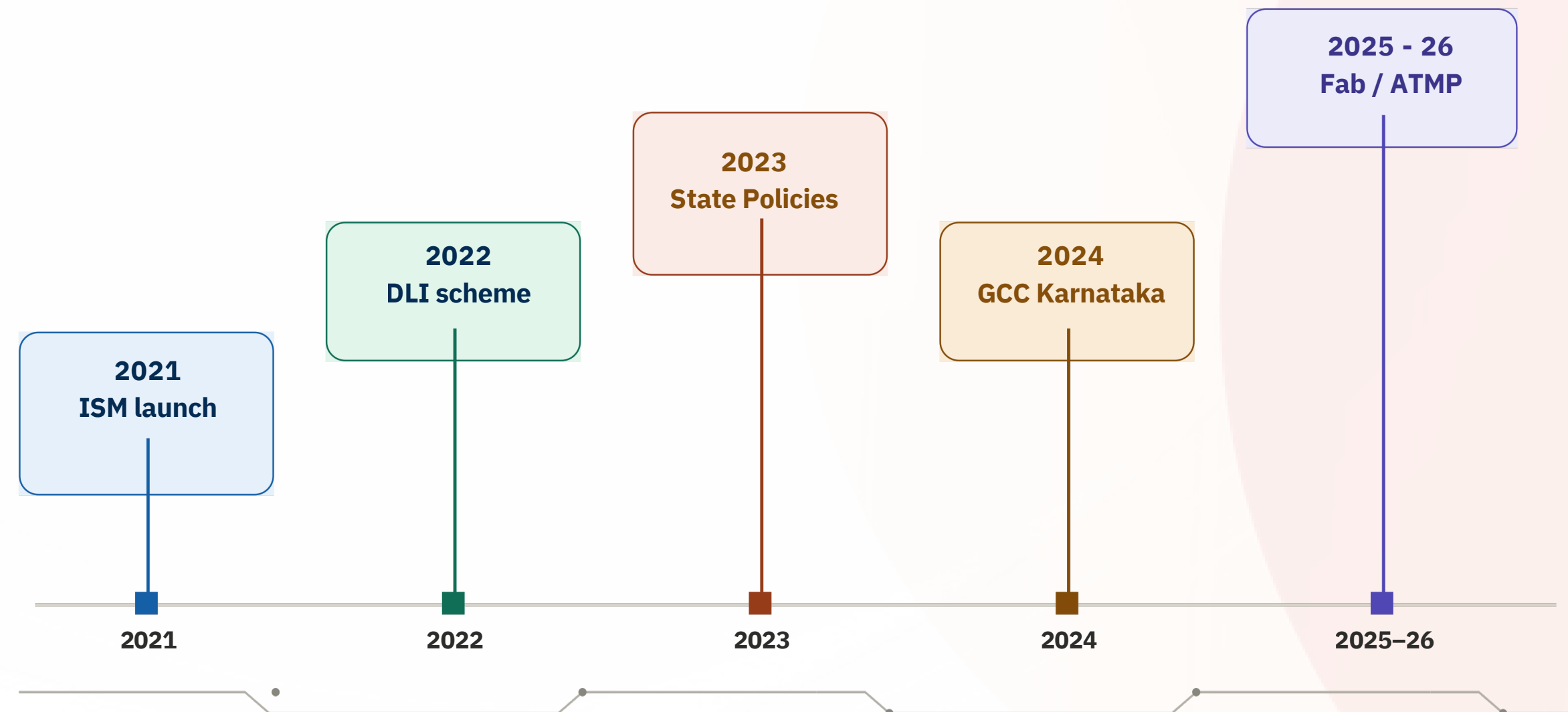
Supporting
Semiconductor Growth



Semiconductor Policy Timeline

INDIA'S CHIP ECOSYSTEM BUILD-OUT, 2021–2026

The timeline outlines key national initiatives, beginning with the 2021 ISM Launch and leading up to critical Fab and ATMP approvals projected for 2025–26. It highlights the strategic, multi-year policy roadmap designed to build and solidify a robust, end-to-end semiconductor ecosystem in India.

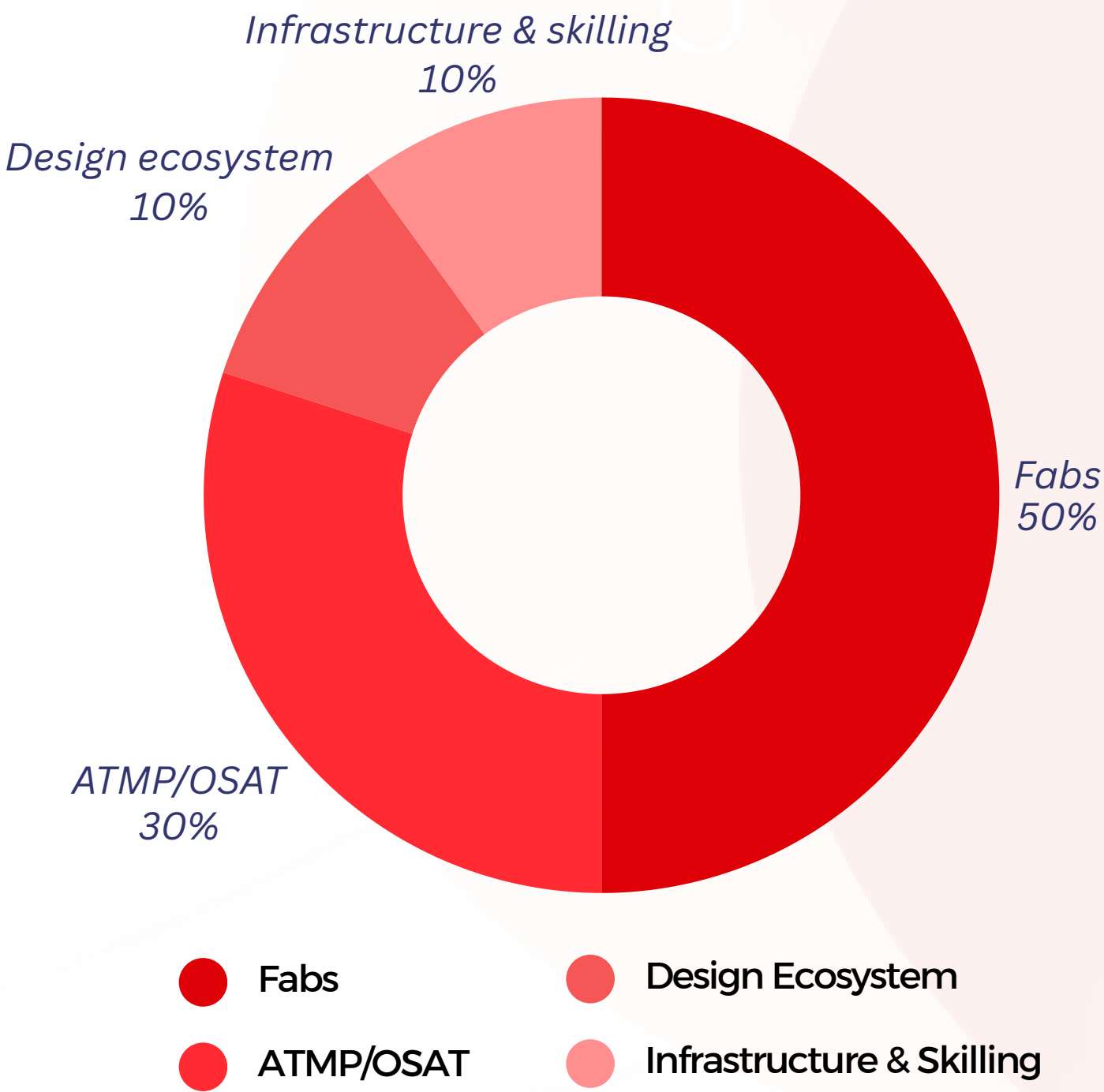


Proposed Semiconductor Fund Allocation (\$10B)

6.1 India Semiconductor Mission (ISM)

The India Semiconductor Mission was launched in Dec. 2021 by the Ministry of Electronics and Information Technology (MeitY) with a ₹76,000 crore (US\$10 billion) incentive package to build a domestic semiconductor ecosystem. The ISM operates under the Ministry of Electronics and Information Technology (MeitY) and provides capital support for fabrication facilities (up to 50 percent of project cost), OSAT/ATMP facilities (up to 30 percent of capital expenditure), and design ecosystem development.

As of early 2026, the ISM has approved the following major investments: Tata Electronics and PSMC (Taiwan) for a 28nm fab in Dholera, Gujarat (USD 11 billion); Tata Semiconductor Assembly and Test (TSAT) for ATMP in Morigaon, Assam (USD 2.9 billion); CG Power and Renesas for ATMP in Sanand, Gujarat (USD 0.74 billion); and Kaynes Technology for ATMP in Sanand (USD 0.46 billion). Micron Technology's ATMP facility in Sanand, receiving partial ISM support, is a separate investment of approximately USD 2.75 billion.



KEY INCENTIVES	EARLY OUTCOMES
Semiconductor fabs: up to 50% fiscal support	Multiple fab and ATMP projects approved under ISM
Display fabs: up to 50% fiscal support	India contributes ~20% of the global semiconductor design workforce
ATMP/OSAT: up to 50% capital subsidy and Design Linked Incentive (DLI) such as, Up to 50% design cost reimbursement, 4–6% incentives on chip sales and Target: 100+ semiconductor startups	Reduce import dependence, strengthen supply-chain resilience, and attract global semiconductor manufacturing investment.

6.2 Design Linked Incentive Scheme

The Design Linked Incentive (DLI) Scheme is a key pillar of the India Semiconductor Mission, implemented by the Ministry of Electronics and Information Technology (MeitY) to strengthen India’s semiconductor design ecosystem. This scheme provides financial incentives for semiconductor design startups and companies developing ICs, chipsets, and embedded software. The scheme offers reimbursement of up to 50 percent of eligible expenditures for design infrastructure (EDA tools, IP licensing) and 6 to 4 percent revenue sharing on net sales for a 5-year period, subject to an overall ceiling. As of 2025, over 35 companies have received DLI approvals, though the scheme has faced criticism for the limited scale of incentives relative to the capital requirements of commercial chip design.

FINANCIAL INCENTIVES	TARGET OUTCOMES
Design Infrastructure Support: Access to EDA tools, IP libraries, and fabrication services.	Support 100+ semiconductor design startups and companies.
Product Design Linked Incentive: Up to 50% reimbursement of eligible design costs and ceiling support per applicant (as per government guidelines).	Encourage development of India-owned semiconductor IP.
Deployment Linked Incentive: 4–6% incentive on net sales of designed chips for 5 years.	Increase domestic chip design and commercialization capability.

6.3

State Government Incentives

Karnataka, Telangana, Maharashtra, Tamil Nadu, and Gujarat have each developed semiconductor-specific industrial policies, offering land allocation, stamp duty exemptions, power tariff concessions, and research infrastructure support. Karnataka's GCC Policy 2024 extends explicit support to semiconductor engineering centers, and Telangana has established dedicated semiconductor parks and VLSI training programs.

STATE	STRATEGIC FOCUS	CAPITAL / PROJECT SUBSIDY	LAND & INFRA SUPPORT	POWER & UTILITIES	TALENT / OTHER INCENTIVES
Gujarat	Semiconductor fabs, ATMP, ecosystem cluster	Up to 40% capex subsidy (in addition to central incentives)	Subsidised land in Dholera SIR, semiconductor park infra, stamp duty reimbursement	Subsidised power tariff, electricity duty exemption	Skill development programs, semiconductor cluster ecosystem
Karnataka	Semiconductor design, R&D, GCCs	Up to 25% capex subsidy	Subsidised land in electronics clusters	Power tariff support	R&D grants, chip design incentives, skilling programs
Tamil Nadu	OSAT/ATMP, electronics manufacturing	Up to 30% capex subsidy	Subsidised industrial land	Reduced power tariffs	Payroll subsidy, workforce training incentives
Telangana	Fabless, chip design, AI chips	Up to 30% project subsidy	Land in Hyderabad electronics manufacturing cluster	Subsidised utilities	R&D grants, startup support, university partnerships
Uttar Pradesh	Semiconductor manufacturing, ATMP	Land subsidy up to 75%, interest subsidy	Dedicated electronics manufacturing zones	Electricity duty exemption	Stamp duty exemption, mega-project incentives
Odisha	ATMP/OSAT, electronics manufacturing	Up to 30% capex subsidy	Subsidised land in electronics parks	Discounted power tariffs	Workforce training, customized mega-project incentives
Maharashtra	Semiconductor design, R&D, manufacturing	Up to 25% capex subsidy	Subsidised industrial land	Reduced electricity tariffs	Mega project packages, GCC/R&D incentives

6.4

Policy Assessment

POLICY DIMENSION	CURRENT STATUS	GAP / EXECUTION CHALLENGE
Fabrication Incentives	50% capital support; projects approved	Long gestation; ecosystem readiness for <7 nm absent
ER&D / Design Incentives	DLI operational; GCC policies at state level	DLI scale insufficient; IP ownership frameworks unclear
Talent Development	VLSI courses, IIT programs, NSDC partnerships	Industry-curriculum alignment weak; faculty shortage
R&D Infrastructure	Chip to Startup (C2S) program; few dedicated fabs	Limited access to advanced process nodes for research
IP Protection	IP regime improved; enforcement gaps remain	Trade secret protection; data localization risks
Export and Trade Framework	Partial alignment with global export control norms	SCOMET updates required for semiconductor equipment

Core Risks

and Structural
Headwinds

A hand with a red glow is pointing at a diagram on a dark surface. The diagram features a central target-like structure with concentric circles and a vertical bar in the center. The word 'RISK' is written on the bar. Surrounding this central element are various icons and lines, suggesting a complex system or network.

RISK

7.1

Risk Matrix

RISK CATEGORY	PROBABILITY	IMPACT	MITIGATION FRAMEWORK
Senior talent shortage (VLSI architects)	High	High	Partner with IITs, specialist upskilling programs, and return programs for the diaspora.
High attrition in GCC engineering roles	High	Moderate	Retention incentives; equity participation; career ladders for technical tracks
Infrastructure deficits (power, connectivity)	Moderate	Moderate	State-level SLAs; dedicated semiconductor parks; backup power mandates
Import dependency (EDA tools, IP cores)	High	Moderate	DLI support expansion, domestic EDA startup ecosystem, and academic licenses
Limited fab capacity for prototyping	High	Moderate	MPW (Multi-Project Wafer) agreements; ISMC fab; international shuttle programs
Global competition for semiconductor talent	High	High	Strengthen domestic compensation benchmarks; immigration reform for returnees
IP leakage and confidentiality risks	Low to Moderate	High	Corporate policy enforcement; legal infrastructure; secure network environments
Geopolitical restrictions on technology	Moderate	High	Engagement in multilateral frameworks; alignment with ITAR/EAR; domestic IP development

7.2

Talent Concentration Risk

India's semiconductor engineering talent is concentrated in four cities and in a narrow band of engineering institutions. Approximately 60 percent of the senior VLSI engineering workforce is located in Bengaluru alone. Any disruption to that geography (infrastructure, policy, or labor market) carries disproportionate risk. Talent distribution to Tier-2 cities (Coimbatore, Mangaluru, and Nagpur) with university-linked semiconductor programs is a structural mitigation that remains underdeveloped.

7.3

Design-to-Silicon Gap

India's semiconductor design community has limited access to physical silicon prototyping, which constrains the transition from design-only capability to full product engineering. Access to advanced process nodes for academic and startup prototyping requires Multi-Project Wafer (MPW) slots at foundries, most of which are located outside India. The absence of domestic advanced-node access lengthens design iteration cycles and imposes cost barriers on smaller design teams and startups.

Market Outlook

and Projections
(2026–2035)



8.1

Growth Projections

SEGMENT	2024 BASELINE	2026E	2028E	2030E
India's Semiconductor Revenue (USD Bn)	55.03	64.45	82.3	108.68
Semiconductor Engineer Headcoun	125,000+	155,000	190,000	235,000 to 250,000
Automotive Semi-Engineers (India)	18,000 to 22,000	28,000	40,000	55,000 to 65,000
AI Chip / Accelerator Engineers	8,000 to 12,000	18,000	30,000	45,000 to 55,000
Semiconductor Startups (cumulative)	120+	200+	320+	450 to 500
India's Share of Global Chip Design Talent	20 to 25%	23 to 26%	26 to 29%	28 to 32%

8.2

Sector-Level Trends

AI Native Chip Architectures

The proliferation of large language models, inference hardware, and edge AI processing is generating demand for AI-specific chip design engineers at a rate that exceeds available supply in the United States and Europe. India's semiconductor sector is well-positioned to absorb a substantial portion of this demand through existing AI engineering teams at NVIDIA, Qualcomm, and Marvell and through the formation of new centers by AI chip startups entering India for the first time. The intersection of chip architecture, compiler development, and model optimization is a competency cluster that Indian engineers are increasingly developing.

India's semiconductor ecosystem is increasingly aligned with global demand for AI and HPC silicon design. Multinational R&D centers and domestic startups are expanding work in AI accelerators, GPUs, and SoC architectures.

Key Indicators

India hosts 150+ semiconductor design centers.	Over 20% of global semiconductor design engineers are estimated to be based in India.
AI inference and training accelerators	Chip architecture and performance modeling.
AI compiler, firmware, and driver stacks.	

Automotive and EV Semiconductor Engineering

The automotive sector is projected to consume USD 200 billion in semiconductors annually by 2030, up from approximately USD 65 billion in 2022. India's automotive OEM and Tier 1 supplier ecosystem (Tata Motors, Mahindra, Maruti Suzuki, Bosch India, and Continental India) is generating domestic demand for semiconductor system integration, functional safety engineering, and embedded software development. This domestic demand, combined with the global automotive semiconductor GCC presence, positions India to develop a self-reinforcing automotive semiconductor engineering cluster.

Key indicators

Rising engineering demand in ADAS, EV power electronics, and vehicle compute platforms.	Automotive SoCs and domain controllers.
Functional safety (ISO 26262) engineering.	Silicon carbide (SiC) and GaN power devices.

Edge AI, Embedded and IoT Silicon Engineering

Edge computing semiconductor demand is driven by industrial automation, smart infrastructure, and consumer devices requiring local processing capability. India's established embedded firmware engineering base is well-suited to support the software stack development, hardware abstraction layer engineering, and power optimization work associated with edge silicon. Companies such as Qualcomm (IoT platforms), NXP (industrial MCUs), and Microchip Technology are expanding India teams to address this segment. India's large embedded engineering base is driving growth in edge computing semiconductor development.

Technology focus areas

Embedded firmware and hardware-software co-design.	Power optimization and real-time systems.
Industrial IoT and consumer device silicon.	Industrial automation.
Smart infrastructure.	Automotive electronics.

Rapid Growth in Chiplet and Advanced SoC Design

Indian semiconductor engineering teams are increasingly contributing to chiplet-based and heterogeneous SoC programs, reflecting the global transition toward modular, multi-die architectures for AI, high-performance computing, and advanced consumer electronics. India's large and mature verification workforce continues to position the country as a global hub for complex SoC verification and integration, particularly for next-generation compute and connectivity platforms.

Key Factors

Growing involvement in multi-die architecture design, integration, and verification.	Development of high-speed interconnect subsystems such as PCIe Gen5/6, CXL, UCIe, and advanced SerDes.
Adoption of AI-assisted verification, emulation, and large-scale validation workflows.	

Advanced Packaging and OSAT Technology Build-out

India is beginning to establish advanced packaging and OSAT/ATMP capabilities, complementing its long-standing strength in semiconductor design and validation. As packaging becomes a critical differentiator for performance, power efficiency, and form factor, demand for packaging engineering talent is increasing. The emergence of packaging and test infrastructure is expanding India's role across a broader portion of the semiconductor value chain.

Key areas

System-in-Package (SiP) and heterogeneous integration.

Reliability engineering, failure analysis, and yield optimization.

Semiconductor test engineering and production validation.

Memory, Interconnect and Data-Center Silicon

India-based teams are playing an expanding role in memory subsystems and high-speed interconnect design that support cloud, hyperscale, and AI infrastructure. These activities reflect India's growing participation in the development of silicon platforms that underpin global data-center and AI computing growth.

Key Factors

Design of DDR5 and High-Bandwidth Memory (HBM) controllers.

Engineering of PCIe, CXL, and next-generation high-speed interfaces.

Storage and server-class silicon validation and performance optimization.

Real-World **Case Studies**



India ER&D Footprint

Intel established its Bengaluru R&D center in 1996, which has grown into the company's largest design and engineering hub outside the United States. Today, India supports global processor programs across client computing, data centers, AI, graphics, automotive, and edge platforms. By 2022, Intel inaugurated a new 453,000 square-foot facility in Bengaluru, its largest design and engineering center outside the United States. Intel operates nine centers in India, eight in Bengaluru and one in Hyderabad.

The Bengaluru center houses engineering teams working across client computing, data center platforms, graphics, IoT, artificial intelligence, and automotive segments. The India workforce spans multiple phases of chip development, from architecture and front-end design to physical design, verification, firmware, and post-silicon validation.



Semiconductor Sub-Functions at Intel India

FUNCTION AREA	CURRENTLY OPERATED	TO-BE EXPANDED
Architecture	Micro-architecture modelling & performance analysis	Greater end-to-end CPU/SoC architecture ownership
RTL Design	Block-level CPU, graphics & interconnect design	Subsystem and full-chip integration leadership
Verification	Functional verification & pre-silicon validation	AI-driven verification and global DV hub role
Physical Design	P&R, timing closure, signal & power integrity	Advanced-node (3nm/2nm) implementation leadership
Silicon Validation	Post-silicon bring-up and debugging	Full platform validation ownership
Packaging	Early packaging collaboration	Chiplet & 3D heterogeneous integration engineering
HW-SW Co-Design	Firmware, drivers, performance tuning	AI PC, data-center & edge platform optimization
EDA & Automation	Tool flows & design automation	AI-assisted design and predictive analytics
Leadership Roles	Growing senior engineering leadership	Global product and program ownership

Why Intel Leverages India for Semiconductor ER&D

India provides the scale, specialization, and cost efficiency required for complex and validation-intensive chip programs.

Key Drivers

Large VLSI, architecture, and verification talent pools.

Mature EDA and GCC ecosystem in Bengaluru.

24-hour global engineering cycle across time zones.

Strong campus hiring pipeline supporting long-term R&D growth.

Semiconductor Capabilities Anchored in India

India teams contribute across the full semiconductor R&D lifecycle and have progressed from support roles to design ownership and platform co-development.

Core Contributions

CPU and SoC design across Xeon and Core processors.	Physical design, verification, and post-silicon validation.
Firmware and low-level platform software engineering.	AI, data-center, and HPC silicon development.
Chiplet and modular architecture workflows.	Advanced packaging and heterogeneous integration validation.

Benefits Gained from India as an ER&D Hub

1. Rapid scaling of large design and verification teams supporting advanced-node and validation-intensive programs.
2. 24-hour engineering cycles across India-US time zones accelerate end-to-end silicon development.
3. Evolution from support roles to design-block ownership and platform co-development.
4. Cost efficiency enables larger teams for complex and modular chip programs.
5. Growing pool of senior architects and engineering leaders supporting global product development.

Key Challenges

Intense competition for VLSI and chip architecture talent.	High attrition in verification and physical design roles.
Need for long-term investment in senior technical leadership.	Cross-time-zone coordination during time-critical tapeout programs.
Organizational uncertainty during global restructuring cycles.	

Mitigation Strategies

35-40% of engineering intake through campus hiring to build long-term pipelines.	Partnerships with IITs and women's engineering colleges to expand talent supply.
Collaboration with the India Semiconductor Mission on training across chip design and packaging.	Academic AI PC experience centers to strengthen ecosystem engagement.
Internal mobility and global program exposure to improve retention.	

India ER&D Footprint

Micron Technology established its India operations in Bengaluru and Hyderabad, building a strong engineering presence focused on memory and storage technologies. The India centers evolved from product engineering and IT support roles into end-to-end R&D for DRAM and NAND memory solutions.

Micron is simultaneously expanding into semiconductor manufacturing value chain participation through its Assembly, Test, Marking, and Packaging (ATMP) facility in Sanand, Gujarat, reinforcing India's role across the semiconductor lifecycle.

Key Statistics



India Workforce

~3,000+

Employees in India

Majority in engineering roles



Atmp Investment in Gujarat

~\$2.75 BILLION

Announced

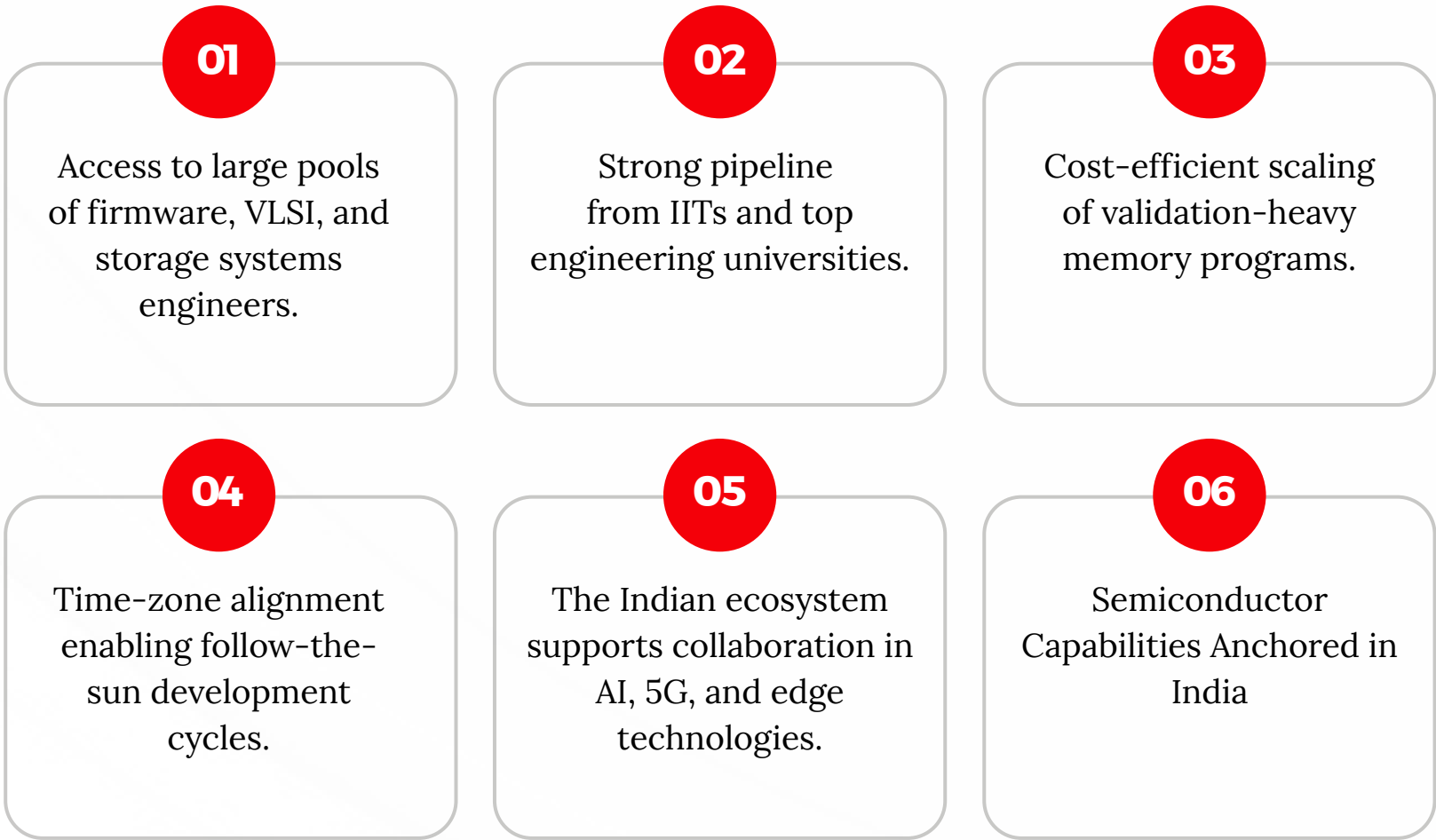
Semiconductor sub-functions at Micron Technology

FUNCTION AREA	CURRENTLY OPERATED	TO-BE EXPANDED
Memory Architecture	DRAM & NAND product engineering support	Greater ownership of memory system architecture and roadmap
Firmware & Storage Software	SSD firmware, embedded storage software	Advanced firmware for AI, cloud and hyperscale storage
Validation & Reliability	System testing, qualification, reliability engineering	Large-scale automation and predictive reliability analytics
Product & Platform Engineering	Client, enterprise and data-center storage solutions	Full platform ownership for next-gen memory systems
AI & Workload Optimization	Performance benchmarking and workload tuning	Memory optimization for AI/HPC and data-intensive workloads
Manufacturing Support	Engineering support for ATMP operations	Advanced packaging engineering and process innovation
Supply Chain & Operations Analytics	Quality, yield and operations analytics	Smart manufacturing and digital factory capabilities
Technical Leadership	Growing senior engineering roles	Expanded global ownership and program leadership

Why Micron Technology Leverages India for Semiconductor ER&D

Micron leverages India for memory architecture, firmware, validation, and storage software, supported by the country’s deep talent pool in computer engineering, embedded systems, and data infrastructure.

Key Points



Micron India plays a critical role in the global development of DRAM and NAND products, spanning silicon to system-level integration.

Key R&D Contributions

- DRAM and NAND product engineering.
- SSD firmware and storage software development.
- Memory validation, reliability, and system testing.
- Data center and client storage platform engineering.
- AI, 5G, and edge-ready memory solutions.
- Enterprise storage and cloud infrastructure enablement.

Benefits Gained from India as an ER&D Hub

- Rapid scaling of firmware and validation engineering teams.
- 24-hour engineering cycle across US-India collaboration.
- Cost efficiency enabling large tests and reliability programs.
- Growing base of senior technical leaders in India.
- Strong collaboration with academia and ecosystem partners.

Key Challenges

- Intense competition for memory and storage engineering talent.
- Attrition in firmware and validation roles across semiconductor firms.
- Need for long-term leadership pipeline development.
- Cross-timezone coordination for product release cycles.

Mitigation Strategies

- Campus hiring and university partnerships to build talent pipelines.
- Collaboration with the India Semiconductor Mission ecosystem.
- Participation in semiconductor manufacturing through ATMP.
- Strong internal mobility and global project exposure.

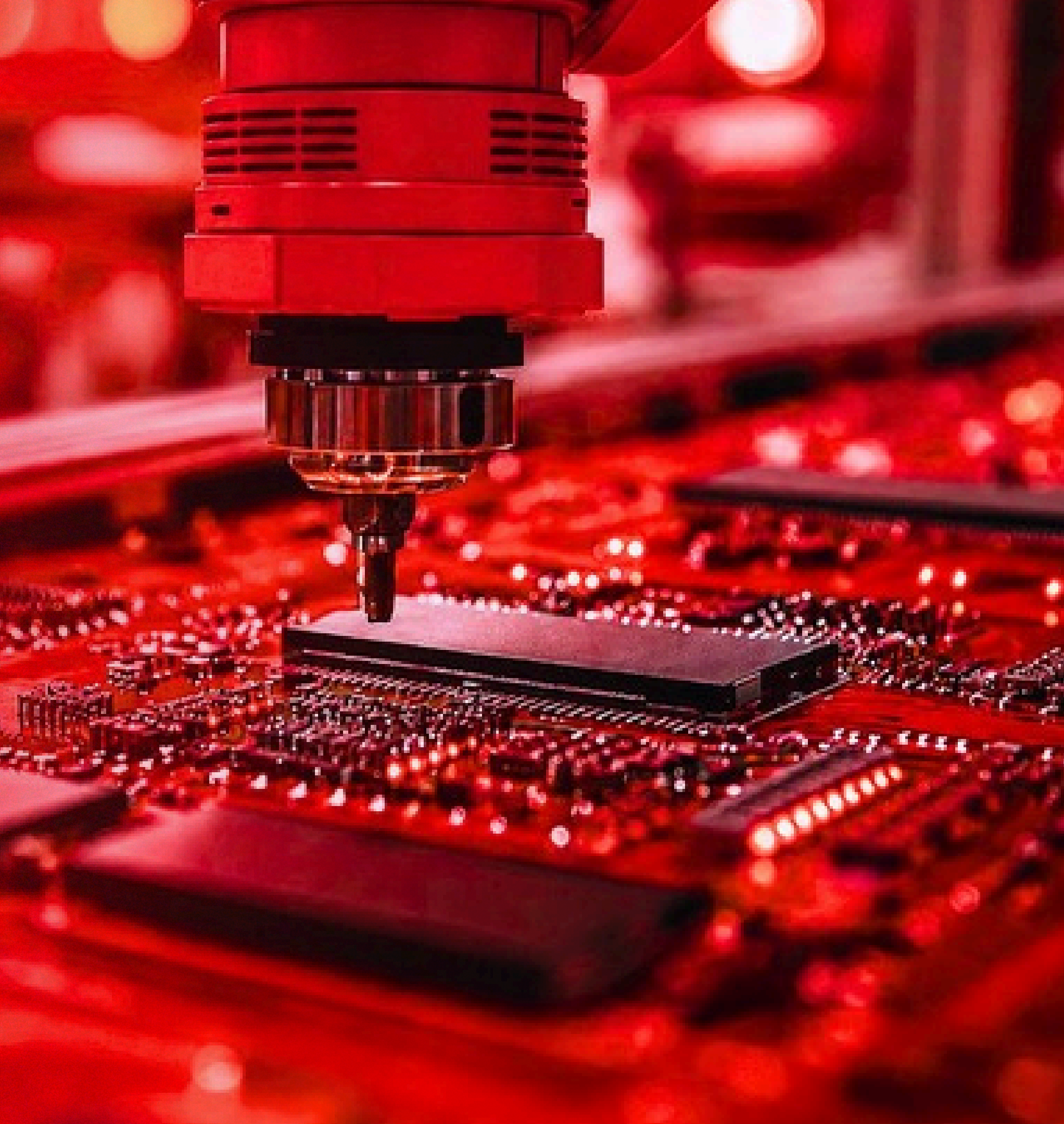
Conclusion

India has firmly emerged as a strategic location for semiconductor engineering, research, and development (ER&D), evolving from a support-led offshore model to a core contributor within global semiconductor value chains. Global Capability Centres (GCCs) in India now participate across architecture, design, verification, firmware, product engineering, software enablement, and manufacturing support, reflecting a clear shift toward end-to-end product ownership.

The evidence indicates that multinational semiconductor firms are steadily expanding India's mandates from execution-oriented work to leadership of complex engineering programs, platform development, and long-term technology roadmaps. The scale and quality of engineering talent, the maturity of the ER&D ecosystem, policy support, and strengthened academia-industry collaboration collectively reinforce India's position as a dependable R&D partner.

At the same time, the ecosystem continues to life cycle areas such as advanced manufacturing depth, infrastructure readiness, and senior leadership pipelines. Ongoing investments in semiconductor design centres, ATMP facilities, talent development, and ecosystem partnerships demonstrate sustained confidence in India's long-term role in global semiconductor strategies.

Looking ahead, India is well positioned to become a critical global hub for semiconductor research, design, and engineering. The continued transformation of GCCs into innovation-driven centers will play a central role in shaping India's contribution to the next phase of global semiconductor growth.



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Inductus **GCC** Service Models

— India's Leading GCC Enabler —

BOT (Build-Operate-Transfer)

A structured pathway to establishing your GCC with minimized risk and maximum efficiency. We **build** and **operationalize** your center, ensuring seamless performance before **transferring full ownership** to you—**equipping your business with a mature, self-sustaining capability**.

COPO (Company-Owned, Partner-Operated)

Maintain **full ownership** while leveraging Inductus' operational expertise. This model enables you to establish a GCC with **absolute control over intellectual assets (IP), agility, and scalability** while we manage day-to-day operations, **ensuring zero liability, compliance, and maximum efficiency**.

Additionally, a **Zero Capex Model** with **Digital Twin** or a **Mirror Like Operational Structure** with superior process excellence.

FLEXI (Adaptive & Custom GCC Solutions)

Beyond predefined structures, **Flexi** is a **bespoke model offering absolute customization and adaptability**.

It molds itself around your unique business prerequisites, evolving seamlessly with your vision. **This isn't just a service—it's an agile, high-impact partnership crafted to maximize your success.**

Proud recipient of **Times Power Icons Award**
for being one of the **Leading GCC Enabler of India**

Presented by



Inductus ensures that each model is executed with precision, innovation, and strategic foresight—helping you unlock the full potential of your GCC in India.

Our deep expertise in GCCs, coupled with a strong network of industry partnerships and policy-level advisory, positions us as a trusted partner for driving transformational outcomes.

Certificate of Excellence for Consulting & Advisory Services
by **Chicago Open University USA**



COPPO & Digital Twin Integrated Service Model

A study based proposition to build a global standard GCC mechanism for Large & Mid-sized Corporations



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"In a world full of rapid tech & process disruptions, global corporations that invest in innovation-led R&D don't just survive—they lead. Innovation is the key to staying relevant, cost-competitive, and future-ready in an ever-evolving marketplace..."

— Alouk Kumar - CEO, Inductus —

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Inductus GCC's Digital Twin and COPPO (Company-Owned, Partner-Operated) Service Model creates a seamless, future-ready operational framework for global businesses setting up GCCs in India. The Digital Twin Process ensures real-time collaboration, decision-making, and operational efficiency by replicating physical systems in a virtual environment, enabling synchronized execution across multiple time zones. Meanwhile, the COPPO Model allows MNCs to retain full ownership and strategic control while leveraging Inductus' expertise for execution, compliance, and scalability.

This hybrid approach optimizes costs, mitigates risks, and accelerates GCC growth, ensuring innovation-driven operations with minimal liabilities and maximum efficiency.



Designed to be Different.

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